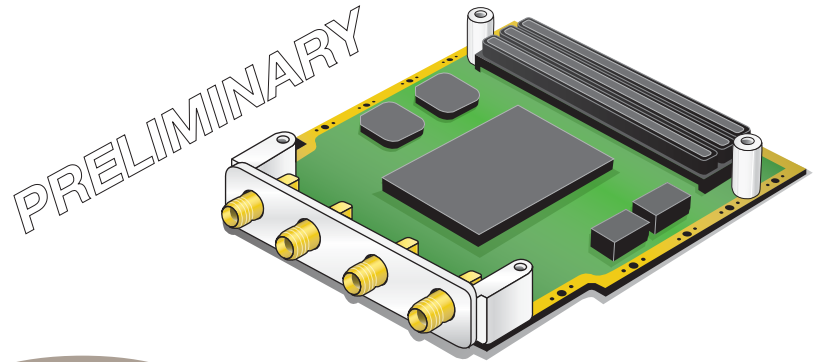




Real Time, High Performance Acquisition Solutions



Features

- Dual Channel 1.6Gsps, 12-bit ADC
- Single Channel 3.2Gsps, 12-bit ADC
- 2.8GHz input bandwidth
- FMC/VITA 57 Form Factor

Benefits

- Best dynamic range over 1Gsps
- Works with Altera & Xilinx FPGA's
- Industry standard form factor
- Rugged and Reliable

Performance

- 150Msps to 1600Msps sampling rate
- Up to 2.8GHz Input Bandwidth
- ENOB=8.6 Effective Bits, $F_{IN}=1448\text{MHz}$
- 4 channels in single VME/VXS/VPX Slot

Overview

The ADF-D1600 leapfrogs Delphi Engineering's (DEG) previous Analog-Digital converter products that were based on National Semiconductor ADC's. DEG engineers designed this product to support the ADC12D1000, ADC12D1600 and the ADC12D1800 devices enabling customers to select their sample rate optimized for their application & obtain the best dynamic performance. The ADF-D1600 provides the highest conversion resolution for sample rates above 1Gsps. This FPGA Mezzanine Card (FMC) converts two channels of up to 2.8GHz analog input bandwidth at 1.6Gsps and 12-bit resolution. Based on the VITA 57 specification, the ADF-D1600 enables direct coupling of unparalleled analog-digital conversion capability with the VME/VXS/AMC/VPX/PCI-E carrier board of your choice. DEG engineers have designed this product and associated HDL firmware to work with both Altera and Xilinx FPGA's.

DEG engineers leveraged design work and intellectual property from the highly successful ADF-2500 board to bring the ADF-D1600 to market in record time. By coupling this core architecture with the compact and flexible FMC form factor, DEG has enabled customers to rapidly and cost-effectively build compact & rugged systems with 2-4 channels of high-speed digitization in a single high performance processor/carrier board. This flexible approach reduces overall power consumption footprint and cost while increasing ruggedness and reliability.



ADF-D1600 Details

The front panel of the ADF-D1600 has four 50Ω connections. They are ports for analog sources, clock input or external reference clock and trigger input.

Analog Input

Each analog input is single-ended with a full-scale input of 800mVpp. The analog input signal bandwidth extends up to 2.8GHz. Software-controllable attenuation may be available for select customers. Maximum input is 2Vpp.

Clocks

The user can provide a clock signal or use the on-board synthesizer to provide the clock. The clock input allows frequencies between 150MHz and 1600MHz.

Reference signal must be a sine or square wave with amplitude from 200mVpp to 3Vpp. Frequencies between 10 and 100MHz are allowed (in 10MHz increments).

The three following sources can be selected for the synthesizer.

- Onboard reference is 1ppm accurate in the entire temperature range of the product
- Front panel clock input
- Carrier reference through FMC connection. This enables board synchronization without external cabling

Triggers

Trigger input must be 200mV to 3.3V peak-to-peak signal. Rise time of less than 10 nanoseconds is recommended. A trigger event is initiated by a positive transition on the trigger input. At the end of a capture event the trigger circuitry is reset to wait for another trigger event. An auto-trigger function enables signal capture without an external trigger.

Trigger input is AC-coupled. DC coupling is available for select customers. Trigger threshold is software

controllable in wide range for both DC and AC coupled versions of the product.

ADCLink

FMC modules are distinct and separate from the FPGA devices that support them. Initiation and control of the ADF-D1600 is accomplished with ADCLink. Board support packages are required for each unique host card.

The capabilities of ADCLink include: clock phase adjustment, onboard/external reference clock control trigger input delays and thresholds, sampling delay adjustments and variable ADC gain.

ADF-D1600 Performance Specifications

Analog Specification	
Number of Channels	2
Sampling Rate	150Msps - 1600Msps
Input Bandwidth	Up to 2.8GHz
Input Impedance	50Ω , AC coupled
Full Scale Input	Single-Ended, 800mVpp
Maximum Input	2Vpp
SNR (Typical)	55dB @ $F_{in}=1448\text{MHz}$
SFDR (Typical)	61.9dBc @ $F_{in}=1448\text{MHz}$
ENOB (Typical)	8.6 Effective Bits @ $F_{in}=1448\text{MHz}$

Clock & Trigger Specifications	
Connectors	50Ω, AC coupled
Clock Input	50Ω, AC coupled
Clock Input Frequency	150 - 1600MHz
Internal Clock	200MHz \pm 1ppm
Std PLL Frequencies	150 - 1600MHz
Trigger Input	Single-ended, 50Ω





Product Selection Guide

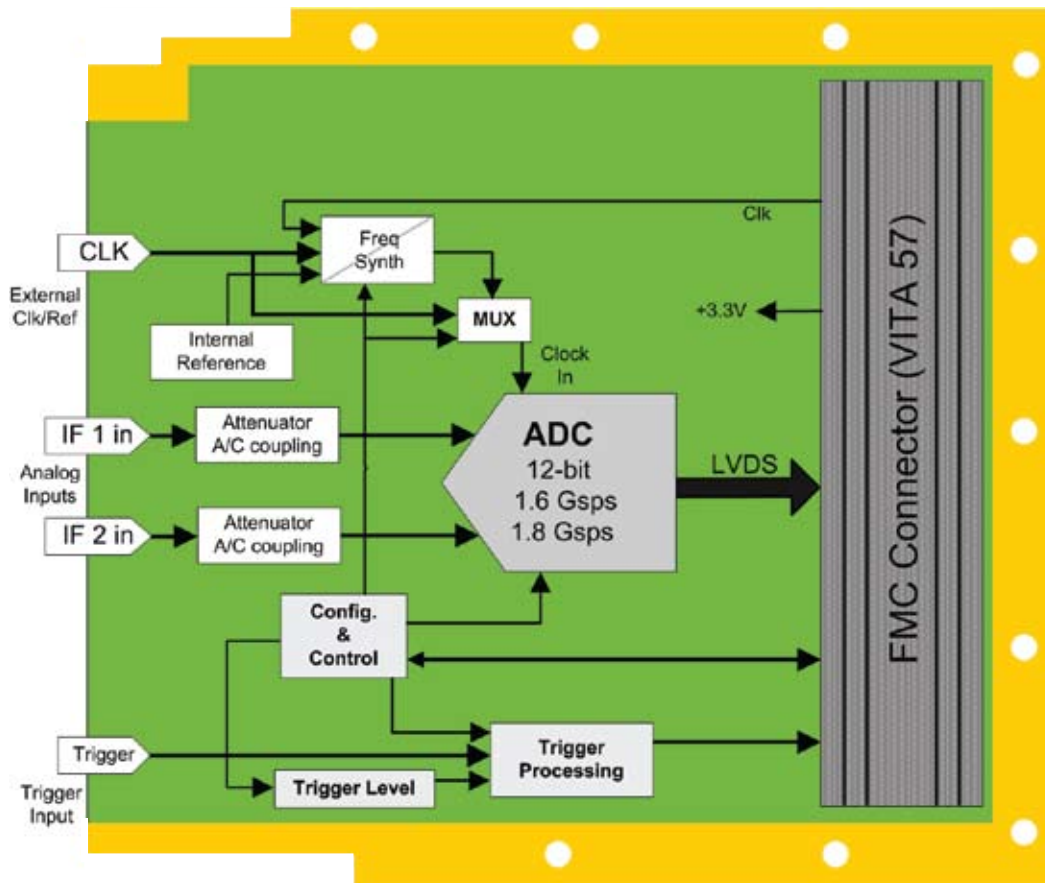
Part Number	Coupling	Rugged Level	Commercial	Rugged	Conduction Cooled	Conformal Coated
ADF-D1600	AC	Commercial	√	-	-	-
ADF-D1600-C	AC	Commercial	√	-	-	√
ADF-D1600-R	AC	Rugged	-	√	-	-
ADF-D1600-RC	AC	Rugged	-	√	-	√
ADF-D1600-CC	AC	Conduction	-	-	√	-
ADF-D1600-CCC	AC	Conduction	-	-	√	√

ADF-D1600 Environmentals

Environmental Specifications	Commercial	Rugged	Conduction Cooled
Operating Temperature	0°C to +50°C (inlet air)	-40°C to +71°C (inlet air)	-40°C to +71°C (at card edge)
Storage Temperature	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C
Humidity (non-condensing)	0 to 95%	0 to 100%	0 to 100%
Vibration (Random)	0.01g ² /Hz 15-2,000Hz	0.04g ² /Hz 15-2,000Hz	0.1g ² /Hz 15-2,000Hz
Shock	20g peak	30g peak	40g peak

Notes: Based on Mil-Spec 810F

ADF-D1600 Block Diagram



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